

Appl. No. 09/813,795
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Amendments to the Specification:

Please replace the paragraph beginning at p. 7, line 8 with the following amended paragraph:

Referring to Fig. 5, the address generation unit 60 is shown in greater detail. A phase accumulator output gradient computation unit 70 operates at $symbol_rate / N$, where $N=4$. Once a slope value has been computed, the additional $N-1$ phase accumulator outputs are obtained by adding the offset values to the current phase accumulator output, as shown. The N phase accumulator outputs are reformatted to generate N look-up table addresses. These N look-up table addresses are then selected consecutively by a multiplexer (Mux) unit 72 to address the look-up table 56. The Mux unit select signal operates at the symbol rate. Figs. 6 and 7 show presently preferred functional configurations for the phase accumulator gradient computation unit 70 and Mux unit 72, respectively. Referring to Fig. 6, the phase accumulator gradient computation unit 70 is shown in greater detail. Adder 100 provides as an output the difference between the output of the phase accumulator 54 and the 'phase accumulator output delayed-by-one-sample', based on the output of the phase accumulator 54. In the presently illustrated example the discrete transform output is provided by inverse Z transform processor 102. At this point, the signals are generated as 16 bit values. The output of adder 100 is a gradient that is provided as input to both hold unit 108 and a magnitude determining unit 104. Magnitude determining unit 104 determines the magnitude of the gradient, and provides the magnitude to comparator 106. Comparator 106 provides a comparison flag as its output indicating whether or not the magnitude of the gradient is equal or in excess of a predetermined threshold Y, which in the presently illustrated embodiment is 100. When the flag output of comparator 106 indicates that the gradient is greater than the predetermined threshold, the comparator output signals to the hold unit to block the high gradient value from being passed to the multiplier 110. The previously computed gradient value is passed instead. This is necessary to prevent incorrect high gradient values (resulting from phase-accumulator wrap-around) from being passed on to the next stage. The hold unit 108, provides the gradient value to multiplier 110 where it is multiplied by a function of η . The value of η is shown in Figure 6 for down-sampling factor equal to 1, 2, 3, and 4 respectively. When the flag output of

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comparator 106 indicates that the gradient is sufficiently high, hold unit 108 provides the gradient value to multiplier 110 where it is multiplied by a function of η . The output of multiplier 110 is used to determine offset values. The first offset value, Offset 1, is a 16 bit representation of the output of multiplier 110. The second offset value, Offset 2, is the 16 bit output of bit shifter 116 which shifts the output of multiplier 110 by 1 bit. The third offset value, Offset 3, is the 16 bit output of adder 112, which sums the output of multiplier 110 and the output of bit shifter 114, which shifts the output of multiplier 116 by 1 bit. Referring to Fig. 7, mux unit 72 is shown in greater detail. The N phase accumulator outputs are provided as $addr_1$ - $addr_4$, which are 16 bit values. $Addr_1$ - $Addr_4$ are provided to format application units 118, 120, 122 and 124 respectively. Each of the format application units converts its respective $addr_x$ value from a 16 bit representation to an 8 bit address value which is then provided to multiplexer 126. Multiplexer 126 is controlled by a 2 bit select signal which sequentially selects the 8 bit addresses provided as input. The output of multiplexer 126 is then sent to the symbol-rate look-up table 56. In further reference to Fig. 5, $addr_1$ is the 16 bit phase accumulator output, **ph acc out**. $Addr_2$ is the output of an adder 80 that receives both Offset 1 and the **ph acc out**, as input. $Addr_3$ is the output of an adder 82 that receives both Offset 2 and the **ph acc out**, as input. $Addr_4$ is the output of an adder 84 that receives both Offset 3 and the **ph acc out**, as input.

Please replace the paragraph beginning at p. 7, line 17 with the following amended paragraph:

Referring to Fig. 8, an example of the phase accumulator output once carrier lock has been achieved is shown. In the example, a down-sampling factor of $N=4$ is used. The phase accumulator outputs at the down-sampled rate are referenced at 80. The expected phase accumulator output is a quantized sawtooth, as shown by the dashed line 82. Therefore, the gradient, or slope, between the down-sampled outputs can be determined, as shown in Fig. 6, and a linear extrapolation based on the determined slope can be used to extrapolate the $N-1$ extrapolated outputs 84 (i.e. three in the example shown). The combination of the actual phase accumulator outputs 80, at the down-sampled rate, and the extrapolated outputs 84 provide an extrapolated phase accumulator output at the original symbol rate used to generate addresses for input to the look-up table.